Request for Continuing Examination
SN 10/697,406

AMENDED CLAIMS

This listing will replace all prior versions of the claims in the application.

1. (currently amended) A method for optimizing ~~the~~ timing performance of an overall logic circuit where that overall logic circuit is implemented in a Field Programmable Gate Array (FPGA) with <u>at least one</u> programmable interconnect of the FPGA behaving in a way such that ~~the~~ timing of logic signals routed by the programmable interconnect from a specific source to a specific load within the FPGA is affected negligibly by fanout to other ~~logic~~ loads connected to the same source ~~signal~~, the method comprising the steps of:

a) synthesizing the overall logic for <u>a</u> first implementation in ~~an~~ the FPGA, the synthesis including construction and <u>a</u> first placement of ~~the~~ <u>one or more</u> logic functions on the FPGA,

b) analyzing the timing <u>paths</u> of the first implementation with the first placement,

c) determining ~~the most~~ <u>one or more</u> critical timing paths from analysis of the first implementation,

d) selecting as an object for improvement a specific critical <u>timing</u> path from the ~~most~~ critical timing paths,

e) implementing in another way the critical logic in the ~~chosen~~ <u>selected specific</u> critical <u>timing</u> path with <u>the</u> implementation of the critical logic performed with relative disregard as to the fanout of signals to other ~~logic~~ loads in the overall logic circuit and with the placement of logic <u>functions</u> in the chosen critical path designed primarily to minimize the interconnected routing

2

distance of the signals contributing to that chosen critical path, such

~~change~~ <u>implementation being operatively substituted for the first placement</u>

<u>and</u> being a ~~change in the~~ selection of <u>new</u> logic elements ~~and the~~

~~placement of these elements which~~ <u>to</u> implement the critical path, with

said selection of new <u>logic</u> elements ~~allowing for the chosen new logic~~

~~elements to be a simple duplication of the logic gates utilized in the original~~

~~implementation but with placement of those new logic elements more~~

~~optimal than the original~~ <u>being a duplication of the logic elements utilized in</u>

<u>the first placement but forming a second placement of the logic functions</u>

<u>on the FPGA, those new logic elements of the second placement placed in</u>

<u>a more optimal placement than the first placement</u> for minimizing the

interconnected routing distance of the chosen critical path.

2. (previously amended) The method of Claim 1 in which the implementation of

the critical logic in a new way in step e) is limited only to changes in the placement

of the logic elements in the chosen critical path.

3. (currently amended) ~~A method for optimizing the timing performance of an~~

~~overall logic circuit where that overall logic circuit is implemented in an FPGA with~~

~~at least one programmable interconnect of the FPGA behaving in a way such that~~

~~the timing of logic signals routed by the programmable interconnect from a specific~~

~~source to a specific load within the FPGA is affected negligibly by fanout to other~~

~~logic loads connected to the same source signal, the method comprising the steps~~

~~of:~~

3

a) ~~synthesizing the overall logic for a base implementation in an FPGA, the synthesis including construction and placement of the logic functions on the FPGA,~~

b) ~~analyzing the timing of the base implementation,~~

c) ~~determining the most critical timing paths from analysis of the base implementation,~~

d) ~~selecting as an object for improvement a chosen critical path from the most critical timing paths,~~

e) ~~implementing in another way the critical logic in the chosen critical path with implementation of the critical logic performed with relative disregard as to the fanout of signals to other logic in the overall logic circuit and with placement of logic in the chosen critical path designed primarily to minimize the interconnected routing distance of the signals contributing to that chosen critical path, such change being a change in the selection of new logic elements and the placement of those elements which implement the critical path,~~

<u>The method according to claim 1 further comprising</u>:

a) modifying the second placement of ~~other~~ logic <u>functions</u> in the overall logic circuit to accommodate the changes in placement of the chosen critical path while maintaining approximately the new placement of the critical logic,

b) repeating steps b) through e) <u>of claim 1</u> where the last implementation and placement of the overall logic circuit from step e) <u>of claim 1</u> becomes the

4

Request for Continuing Examination
SN 10/697,406

basis for starting again with this last implementation becoming the base

implementation.

4. (previously amended) The method of Claim 3 in which the implementation of

the critical logic in a new way in step e) is limited only to changes in the placement

of the logic elements in the chosen critical path.

5. (new) A method for optimizing overall timing performance of a logic circuit

comprising:

   a) implementing a logic circuit in an FPGA, wherein the FPGA behaves in a

      way such that the timing of logic signals routed from a specific source to

      a specific load within the FPGA is affected negligibly by fanout to other

      loads connected to the same source;

   b) synthesizing a first arrangement of a plurality of elements in the FPGA to

      form one or more logic functions within the logic circuit, wherein each

      logic function has a first placement in the FPGA;

   c) analyzing the timing path of each logic function in its first placement;

   d) determining a critical timing path from the analysis of the first

      placements;

   e) duplicating one or more of the elements forming the logic function having

      the critical timing path;

   f) placing the duplicated elements in a second placement in the FPGA

      which has a shorter critical timing path than the first placement for the

      logic function having the critical timing path.

5

Request for Continuing Examination
SN 10/697,406

6.   <u>The method of claim 5 further comprising repeating steps c) through f)</u>

<u>where the placement resultant from step f) becomes the timing path used in</u>

<u>step c).</u>

6